

**PATENT APPLICATION**  
**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of

Docket No: Q82851

Bhanu KAPOOR

Appln. No.: 10/711,493

Group Art Unit: 2128

Confirmation No.: 5492

Examiner: Russell Warren FREJD

Filed: September 21, 2004

For: A METHOD FOR GENERATING AND VERIFYING ISOLATION LOGIC MODULES  
IN DESIGN OF INTEGRATED CIRCUITS

**AMENDMENT UNDER 37 C.F.R. § 1.111**

**MAIL STOP AMENDMENT**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated June 29, 2007, please amend the above-identified application as follows on the accompanying pages.